III. CLEAN VERSION OF CLAIMS AMENDED

Please substitute each of the following claims for the corresponding pending claim in this application:

C1 Amd D1

23. (Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region;

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has a thickness permitting Fowler-Nordheim tunneling of charges therethrough;

an electrically conductive control gate having a first portion disposed over the first insulation layer first portion and adjacent to the first insulation layer second portion, and a second portion extending over the second insulation layer third portion, the control gate having a substantially vertical sidewall portion; and

an insulation spacer formed adjacent to the substantially vertical sidewall portion of the control gate;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.

C2 6

28. (Amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

C

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

C2 cont'd

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart regions formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region, and

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion and a second portion, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the control gate first portion is positioned over the second insulation layer first portion and adjacent to the second insulation layer second portion and the control gate second portion extends over the second insulation layer third portion, and wherein each of the control gates has a substantially vertical sidewall portion; and

a plurality of insulation spacers each formed adjacent to one of the substantially vertical sidewall portions of the control gates;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.